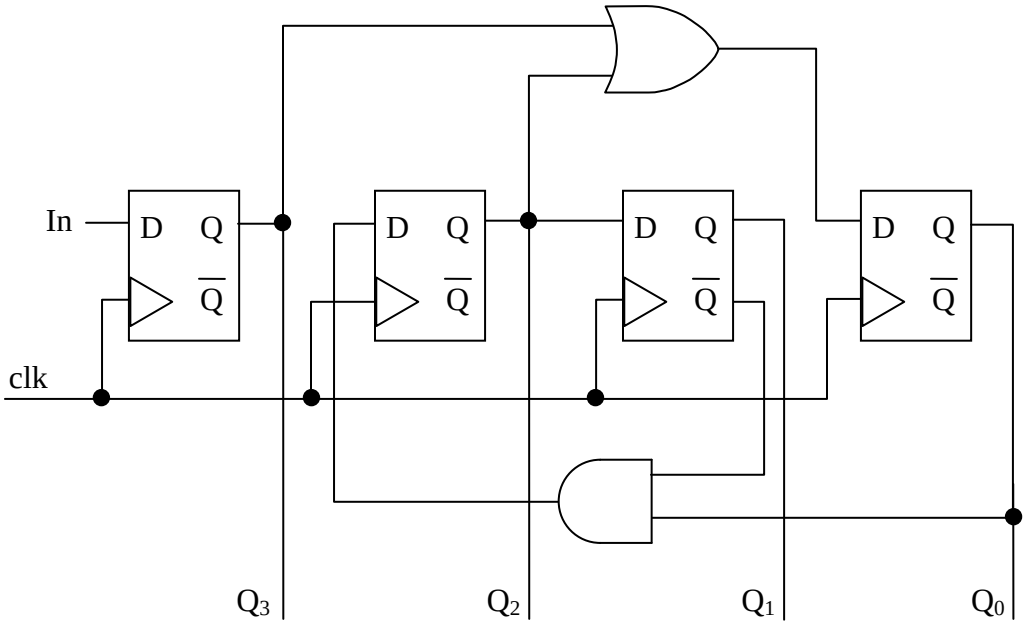
EEE 2243
Digital System Design
Semester II 2011/12

Quiz 1 – 2JKE1

Write the Verilog code for the following circuit:



Correct Answer:

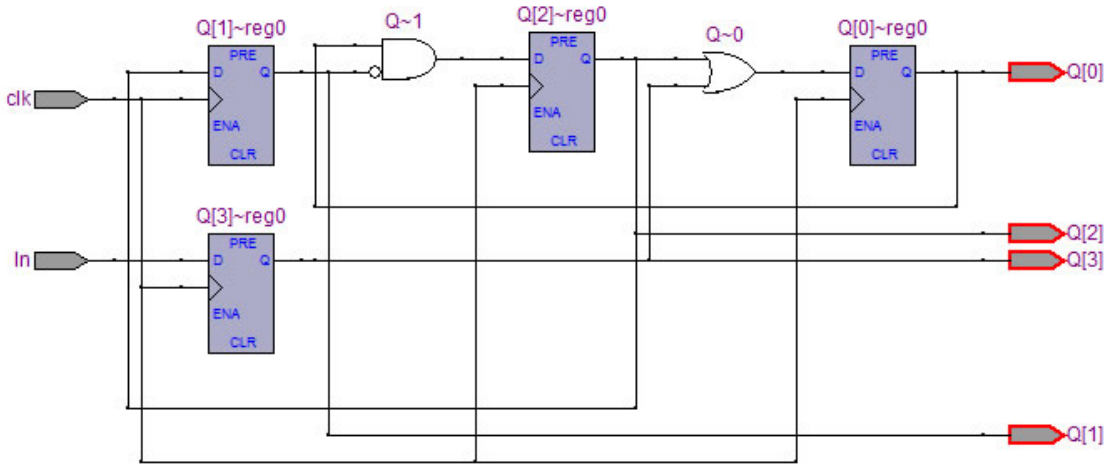
```
module Quiz1_2JKE1_Correct(clk, In, Q);

input clk, In;
output [3:0] Q;
reg [3:0] Q;

always@(posedge clk)
begin
   Q[0] <= Q[3]|Q[2];
   Q[1] <= Q[2];
   Q[2] <= ~Q[1]&Q[0];
   Q[3] <= In;
end

endmodule
```

RTL View:



Wrong Answer:

```
module Quiz1_2JKE1_Wrong(clk, In, Q);

input clk, In;
output [3:0] Q;

assign Q[0] = Q[3]|Q[2];
assign Q[1] = Q[2];
assign Q[2] = ~Q[1]&Q[0];
assign Q[3] = In;

endmodule
```

RTL View: