EEE 2243
Digital System Design
Semester II 2011/12

Quiz 2 – 2JKE2

Write the Verilog code for converting D flip-flop to JK flip-flop.

Answer:

Refer to Chapter 3 slide page 26

By Boolean expression:

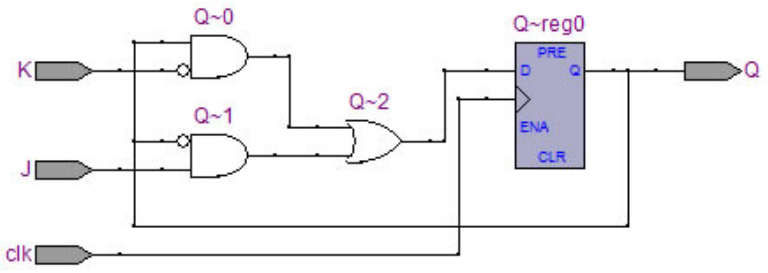
```
module JKFlipFlopBool(clk, J, K, Q);

input clk, J, K;
output Q;
reg Q;

always@(posedge clk)
begin
   Q <= (~K & Q) | (J & ~Q);
end

endmodule
```

RTL View:



By behavioral (two possible solutions):

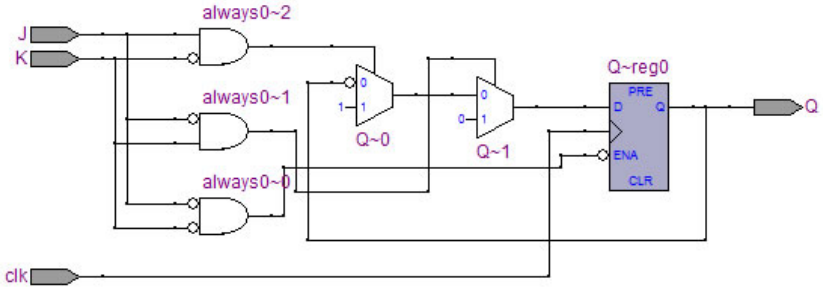
```
module TFlipFlopBeha1(clk, J, K, Q);

input clk, J, K;
output Q;
reg Q;

always@(posedge clk)
begin
   if      ((J == 0) && (K == 0)) Q <=  Q;
   else if ((J == 0) && (K == 1)) Q <=  0;
   else if ((J == 1) && (K == 0)) Q <=  1;
   else                           Q <= ~Q;
end

endmodule
```

RTL View:



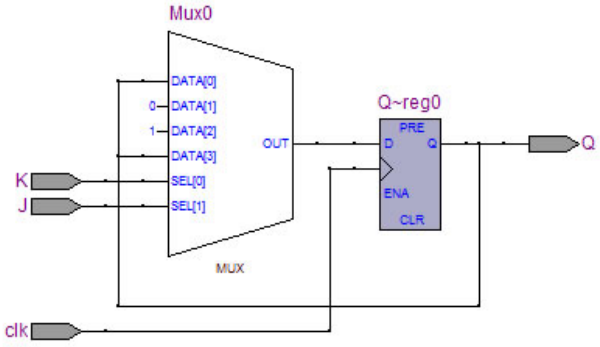

```
module TFlipFlopBeha2(clk, J, K, Q);

input clk, J, K;
output Q;
reg Q;

always@(posedge clk)
begin
   case ({J, K})
      2'b00: Q <=  Q;
      2'b01: Q <=  0;
      2'b10: Q <=  1;
      2'b11: Q <= ~Q;
   endcase
end

endmodule
```

RTL View:


Mux0
DATA[0]
0
DATA[1]
1
DATA[2]
DATA[3]
SEL[0]
SEL[1]
OUT
MUX
Q~reg0
PRE
D
Q
ENA
CLR
K
J
clk
Q