

EEE 2243
Digital System Design
TEST 1 Supplementary

1. a) Write the Verilog code for the following Boolean function WITHOUT minimization using Boolean expression approach: $f = \sum m(0,2,4,5,6,12,13)$
(CO1) [10 marks]

```
0 ⇨      00002
2 ⇨      00102
4 ⇨      01002
5 ⇨      01012
6 ⇨      01102
12 ⇨     11002
13 ⇨     11012

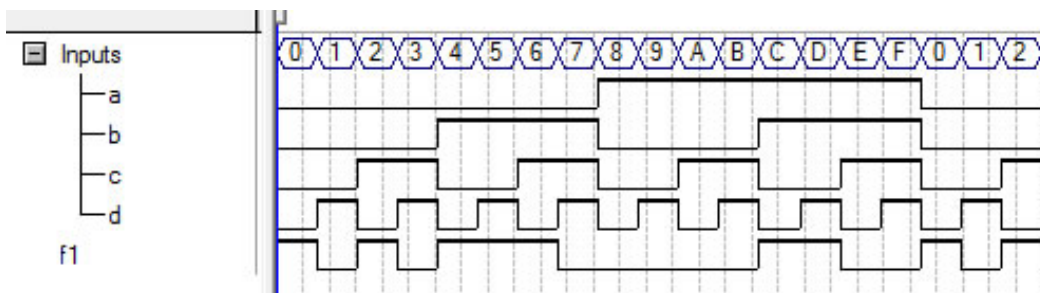
module FuncQ1a(a, b, c, d, f1);

input a, b, c, d;
output f1;

assign f1 =    (~a & ~b & ~c & ~d)
               | (~a & ~b &  c & ~d)
               | (~a &  b & ~c & ~d)
               | (~a &  b & ~c &  d)
               | (~a &  b &  c & ~d)
               | ( a &  b & ~c & ~d)
               | ( a &  b & ~c &  d);

endmodule

Simulation:
```

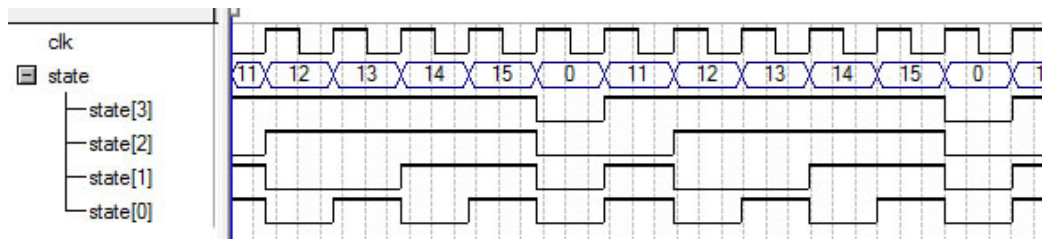


b) Draw the FSM diagram for a 4-bit mod 6 counter starting at 11. Then write the Verilog code for it.

(CO1) [15 marks]

```
module CtrMod6Init11(clk, state);  
input clk;  
output [3:0] state;  
reg [3:0] state;  
  
initial state <= 11;  
  
always@(posedge clk)  
begin  
    if (state == 0)  
        state <= 11;  
    else  
        state <= state+1;  
end  
  
endmodule
```

Simulation:



2. a) Write the Verilog code for the logic circuit in Figure Q2 in Boolean expression approach assuming the initial value of the registers is 101_2 .
(CO1) [10 marks]

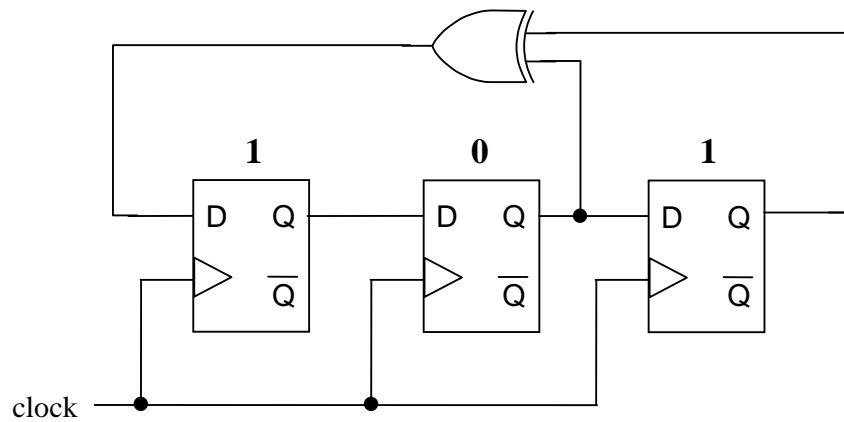


Figure Q2

- b) Construct the state transition table for the same circuit in Figure Q2.
(CO1) [10 marks]
- c) Based on (b), write the Verilog code for the logic circuit in Figure Q2 in behavioral approach.
(CO1) [5 marks]
3. a) Write a Verilog module of 1-bit half-adder.
(CO1) [5 marks]
- b) Instantiate modules of (a) to write a module of 1-bit full-adder.
(CO1) [10 marks]
- c) Instantiate modules of (b) to write a module of 4-bit full-adder with ripple carry technique.
(CO2) [10 marks]
4. a) Explain the steps you use to perform bit-by-bit magnitude comparison.
(CO2) [5 marks]
- b) Write the BOOLEAN expression style Verilog code for the following circuit of a stage of 1-bit magnitude comparator:

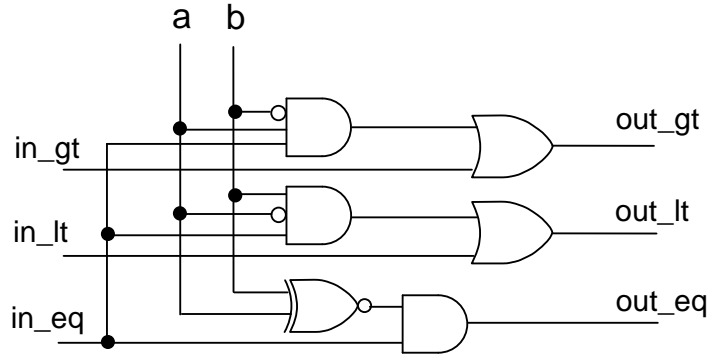


Figure Q4(b)

(CO2) [10 marks]

- c) Figure 4(c) shows a block diagram of a single stage of a bit-by-bit magnitude comparator. Explain (with drawing) how you construct a 4-bit magnitude comparator out of it.

(CO2) [10 marks]

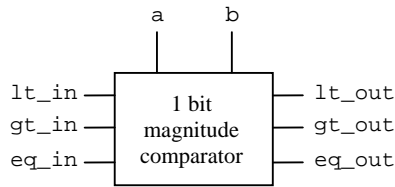


Figure Q4(c)